REMARKS

In accordance with the foregoing, claims 1, 8 and 11 have been amended and claim 2 is cancelled. No new matter is presented and, accordingly, approval and entry of the foregoing amendments are respectfully requested.

STATUS OF CLAIMS

Claims 1-13 are rejected.

Claims 8-10 are objected to but indicated as allowable if suitably rewritten in independent form at page 5 of the Action.

The allowable dependent claim 8/1 is rewritten to independent form, including all of the limitations of its related independent claim 1 and claims 9/8 and 10/9 depend directly and indirectly, respectively, from claim 10; accordingly, claims 8-10 are submitted to be allowable in accordance with the indication of ALLOWABLE SUBJECT MATTER at page 5 of the Action.

Claims 1 and 3-13 are pending and under consideration.

AT PAGE 2 OF THE ACTION: REJECTION OF CLAIMS 1-17 AND 11-13 FOR OBVIOUSNESS UNDER 35 U.S.C. §103(a) OVER APPLICANT'S ADMITTED PRIOR ART IN VIEW OF KURD (U.S. PATENT NO. 6,266,779)

The rejection is respectfully traversed.

Moreover, as noted above, claims 8 and 10 are now in allowable condition and are requested to be withdrawn from the foregoing rejections of claims.

The Examiner concedes at page 2 of the Action that AAPA does not disclose a system resource prescaler as recited by claim 1. Instead, and likewise at page 2 of the Action, the Examiner cites Kurd as disclosing "a system resource prescaler [clock enable generator 110] which generates, from the clock, an operation permission signal [clock enable signal] denoting an operation permissive state in m cycles out of n cycles of the clock [ratio] and supplies the operation permission signal to an internal circuit of an internal resource...."

According to Kurd, in FIG. 1, a clock enable generator 110 outputs clock enable signals to BUS CLOCK macros 120, 130 respectively, and which output common clock signals having a predetermined pulse of core clock CLK according to the clock enable signals, respectively. For instance, in case RATIO=8, the clock enable signal is output at every at every second core clock signal and another at every 8th core clock (CLK) signal (col. 3, lines 28-61).

Therefore, the Applicant assumes that the Examiner alleges that Kurd's clock enable generator 110 corresponds to "the system resource prescaler" of claim 1 and that the clock enable signals could correspond to "the operation permission signal" of claim 1.

However, Applicant respectfully submits that since the bus clock macros 120, 130 do not connect to an arithmetic unit via a bus, it is not obvious and would not have been obvious for a person skilled in the art to add "a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock (m =<n), and supplies the operation permission signal to the internal circuit of the internal resource, where the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state", as recited by claim 1.

According to the invention of claim 1, the microcontroller includes:

> an internal resource... connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit both of which operate in synchronization with the clock; and
>
> a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock (m =<n), and supplies the operation permission signal to the internal circuit of the internal resource,
>
> wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state.

Therefore, the bus control between the microcontroller and the internal resource via the bus can be operated at a high speed rate in synchronization with the clock, whereas the internal circuit within the internal resource can operate at a lower speed rate but in synchronization with the clock. This is an unpredictable, highly beneficial result, yielded by the microcontroller of both claims 1 and 11.

Applicant respectfully submits that independent claims 1 and 11 would not have been rendered obvious under 35 U.S.C. §103(a) over AAPA in view of Kurd, because the reference does not teach or suggest how the clock enable generator 110 and the clock enable signals are applied to AAPA and, moreover, the invention of claims 1 and 11 have the above unpredictable result.

Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-7 and 11-13.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: January 23, 2008

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